

FIG. 1

FIG. 2 is a block diagram of a system 200 for processing a data packet. The system 200 includes a clocking signal input 110, a data packet input 112, and a routed data output 116. The system 200 is implemented on a silica on silicon substrate 104. The system 200 includes a clocking signal input 110, a data packet input 112, and a routed data output 116. The system 200 is implemented on a silica on silicon substrate 104. The system 200 includes a clocking signal input 110, a data packet input 112, and a routed data output 116. The system 200 is implemented on a silica on silicon substrate 104.

200

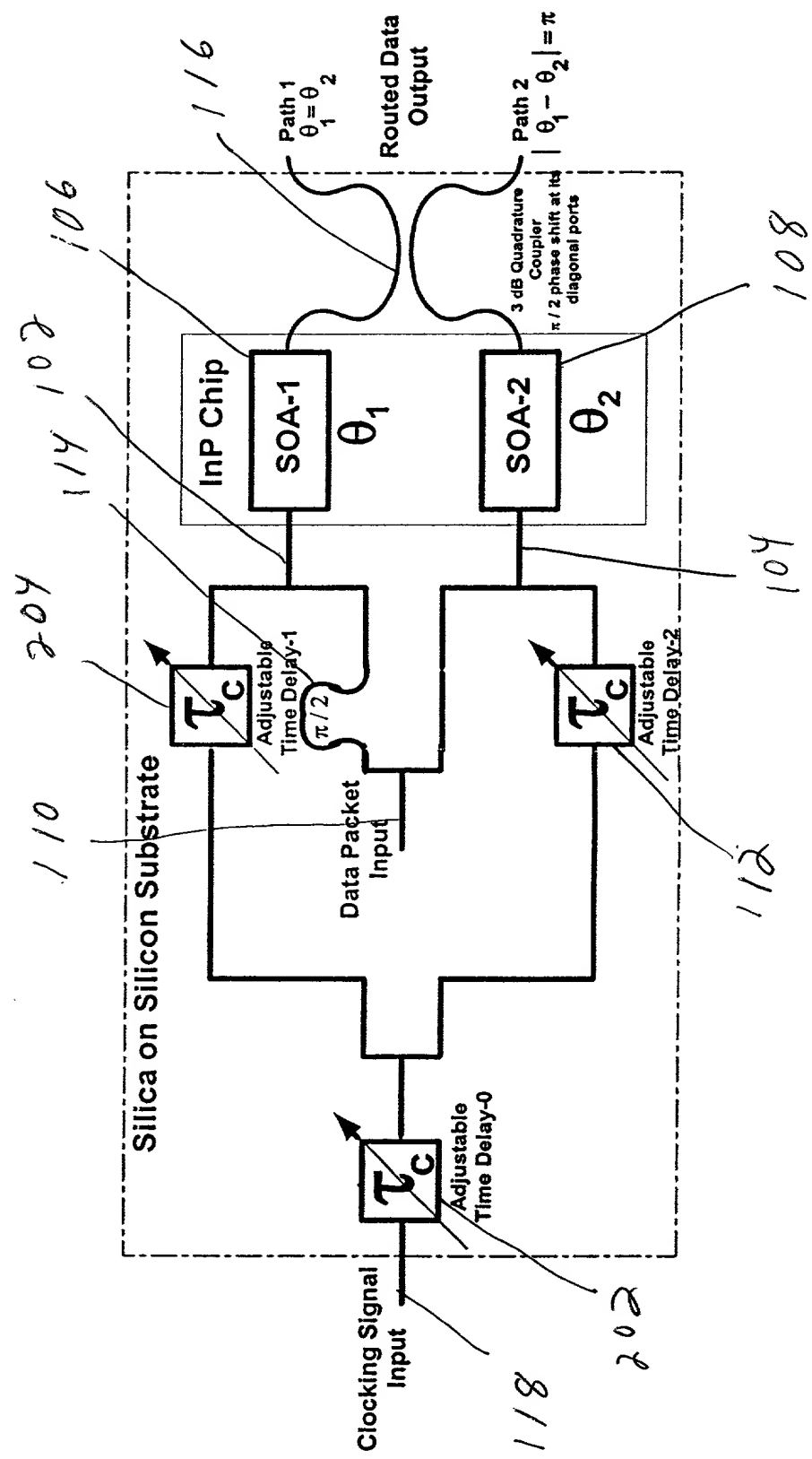


FIG. 2

300

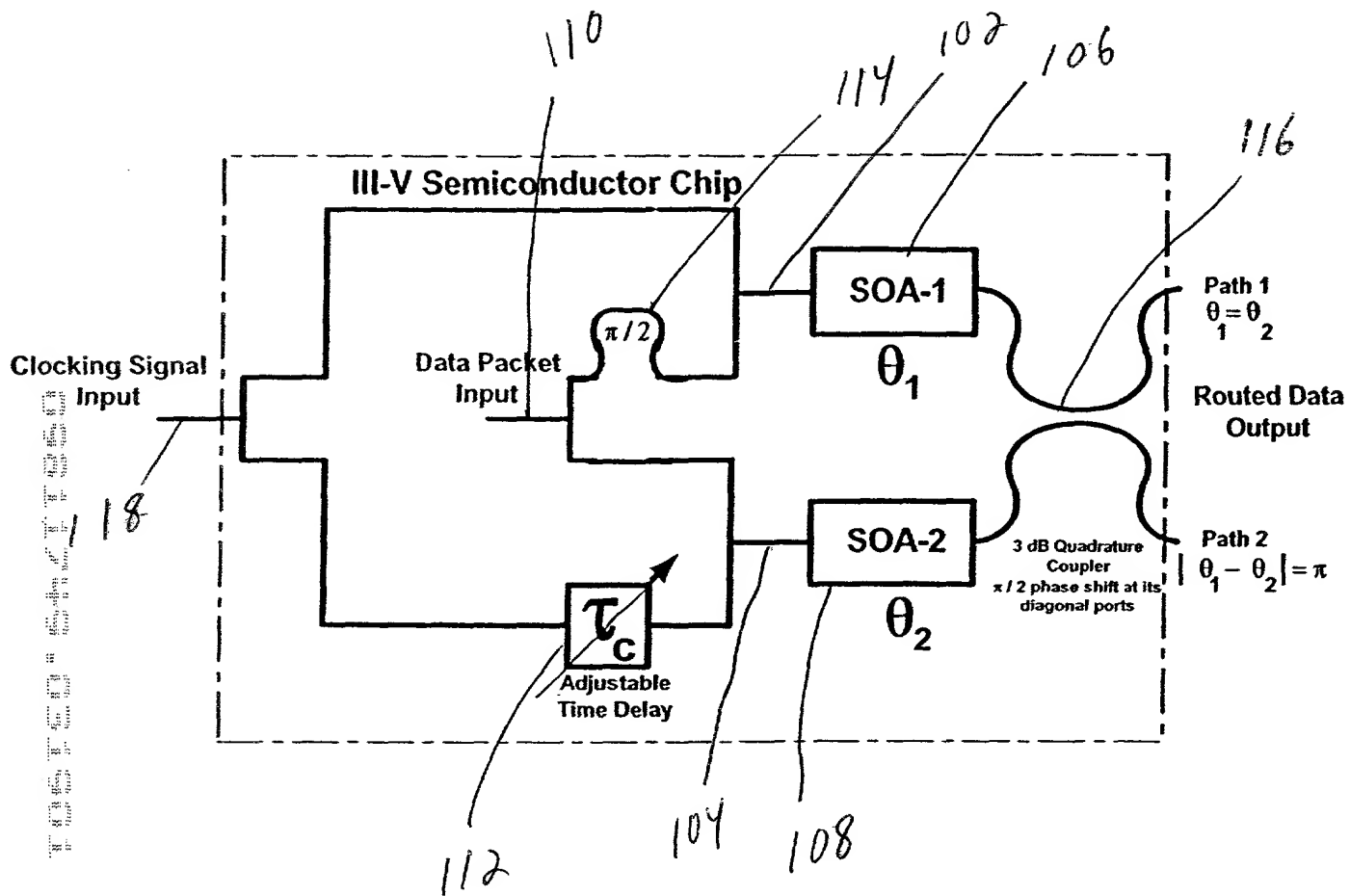


Fig. 3

400 110 204 114 102 106

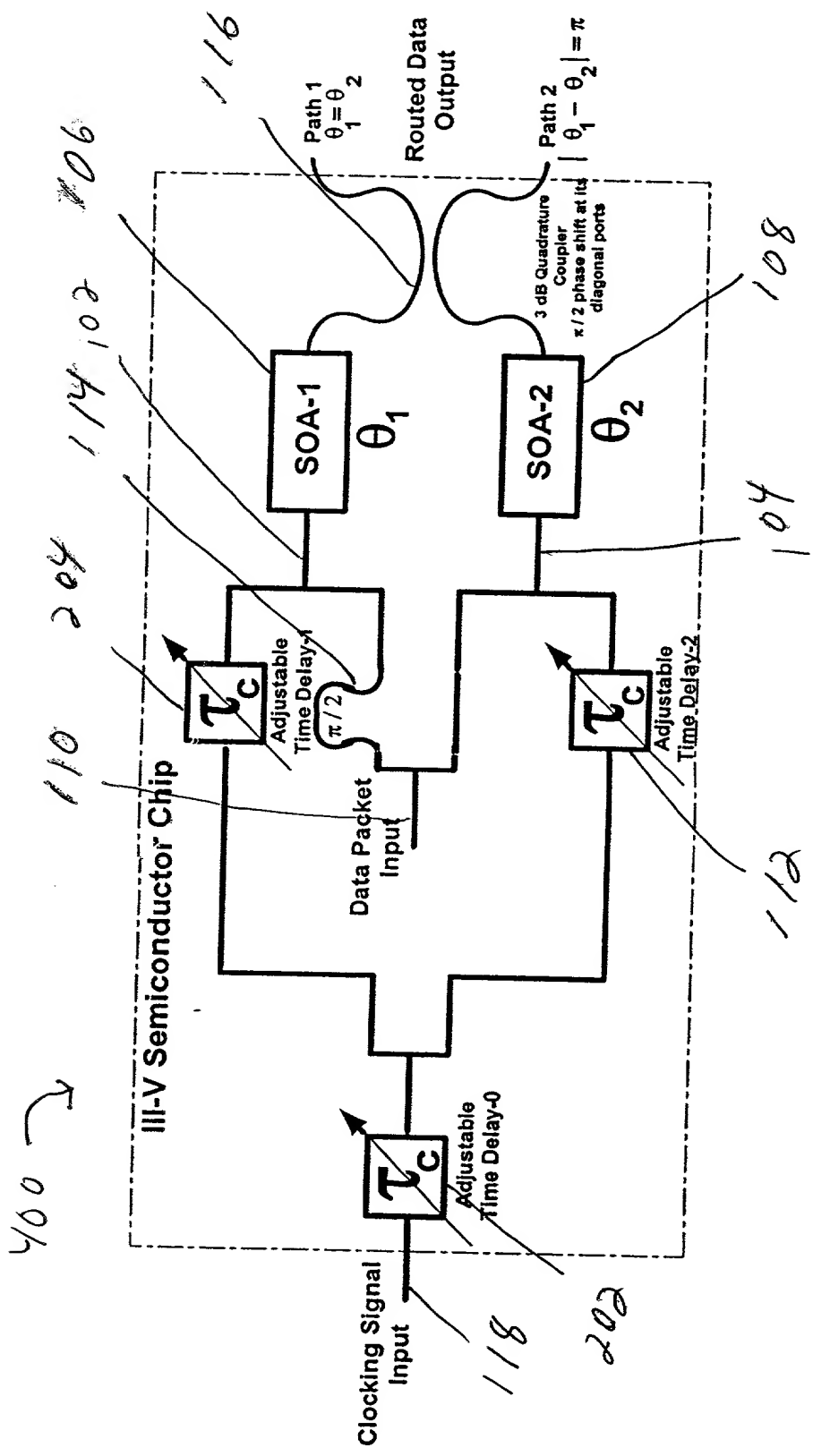


FIG. 4

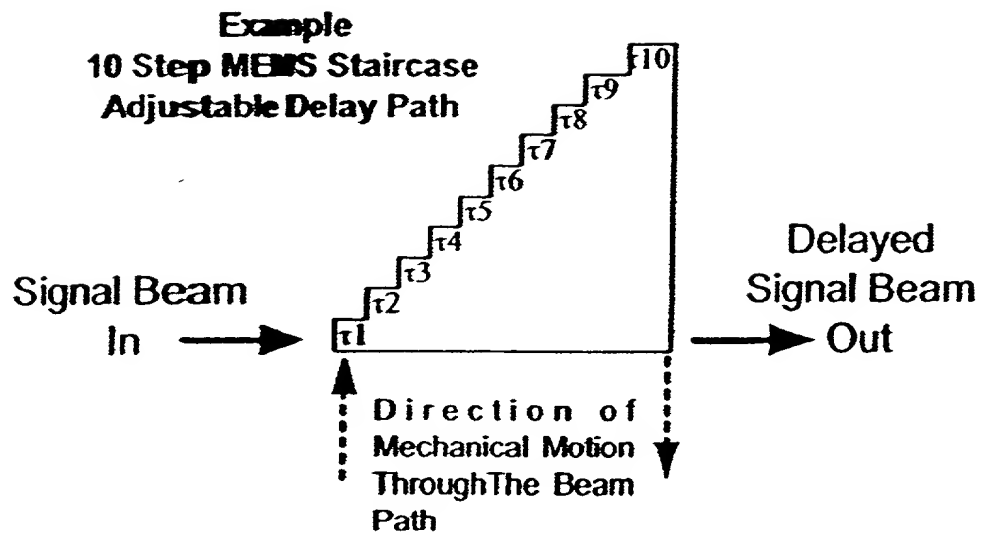


Fig. 5

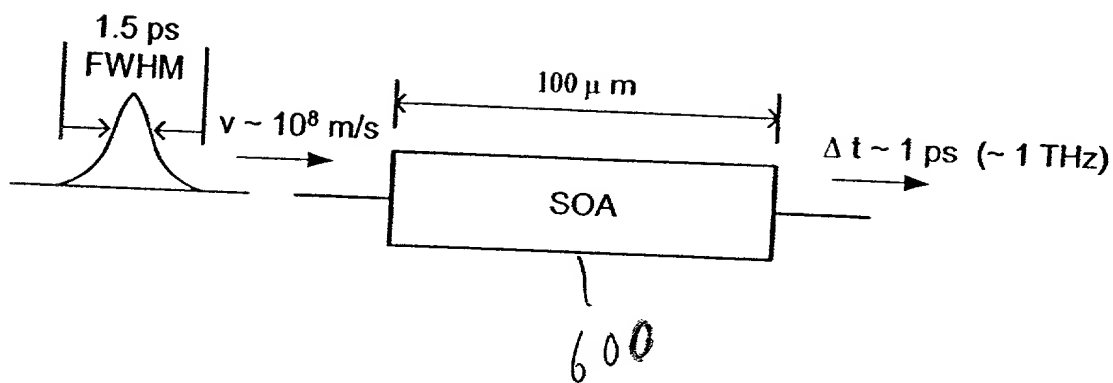


FIG. 6

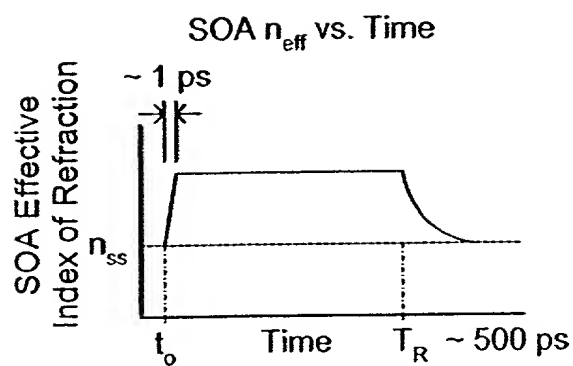


Fig. 7

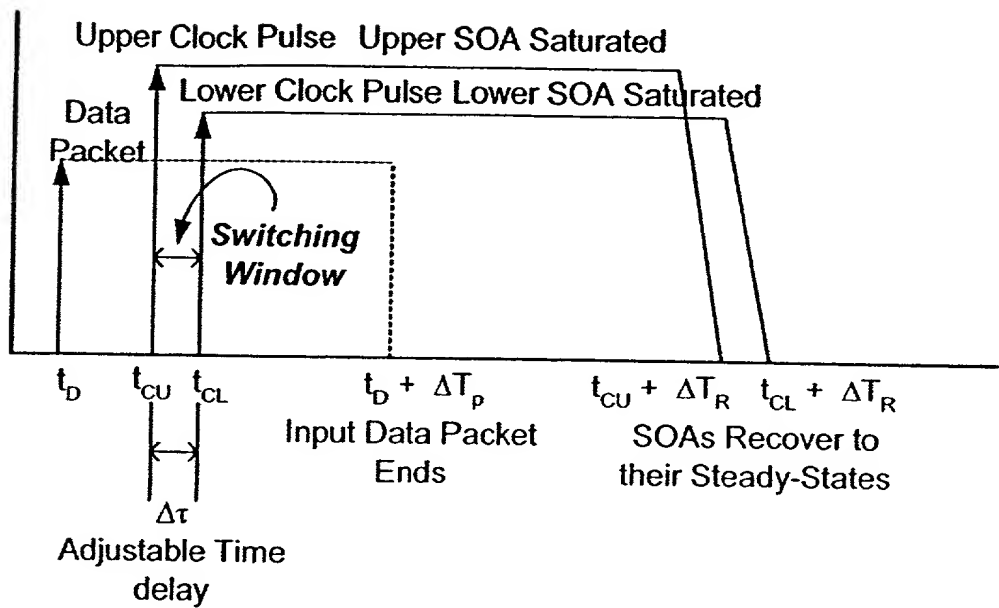


FIG. 8



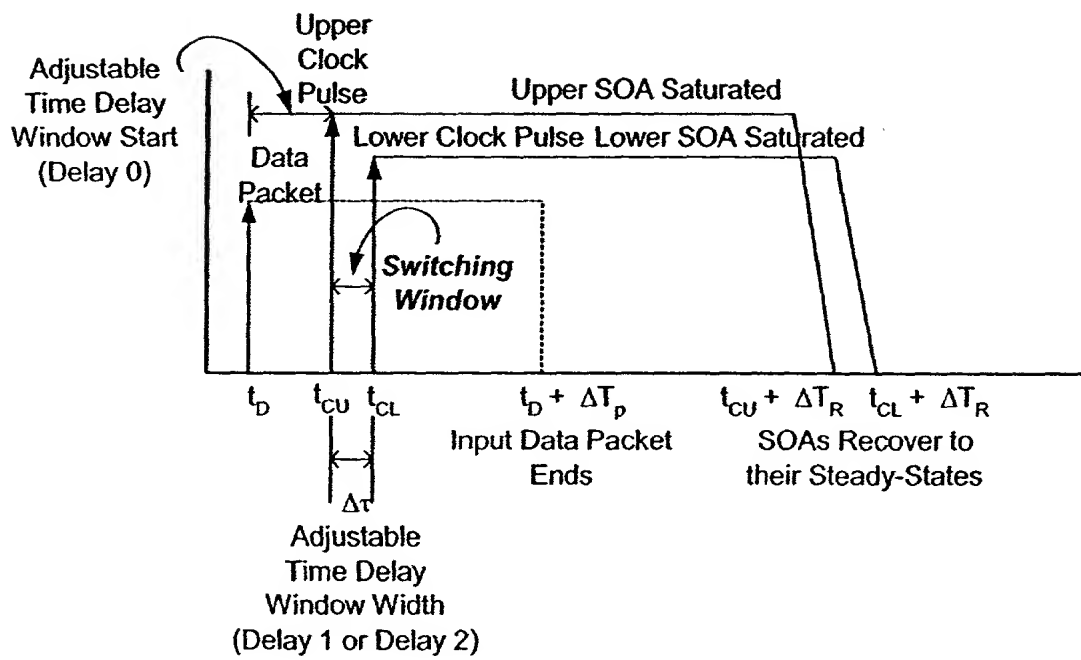


Fig. 9